

Listing of Claims:

This listing of claims is for the convenience of the Examiner. No amendments are made to the claims herein.

1 Claim 1. (*Original*) An apparatus, comprising:
2 a direct memory access register adapted to hold a descriptor, said register comprising:
3 a command register comprising a compare enable bit and a branch enable bit;
4 a source address register;
5 a target address register; and
6 a descriptor address register.

1 Claim 2. (*Previously Presented*) An apparatus as in claim 1, wherein said compare enable
2 bit is adapted to indicate a comparison operation to be performed by a direct memory access
3 controller based on said source address register and said target address register.

1 Claim 3. (*Previously Presented*) An apparatus as in claim 1, wherein said branch enable
2 bit is adapted to indicate a branch operation to be performed by a direct memory access
3 controller to access another descriptor.

1 Claim 4. (*Original*) An apparatus as in claim 1, further comprising a control status
2 register, said control status register comprising a compare status bit.

1 Claim 5. (*Previously Presented*) An apparatus as in claim 4, wherein said branch enable

2 bit is adapted to indicate a branch operation to be performed by a direct memory access
3 controller to access another descriptor based on said compare status bit.

1 Claim 6 (*Withdrawn*) A system, comprising:
2 a target;
3 a source;
4 a memory adapted to contain a first descriptor of a first type, a second descriptor of a
5 second type, a third descriptor of a third type, and a fourth descriptor of said first type;
6 a direct memory access controller coupled to said memory, said direct memory access
7 controller adapted to transfer data from said source to said target based on said first descriptor,
8 said direct memory access controller comprising a direct memory access register to hold said
9 first descriptor, said second descriptor, or said third descriptor, said direct memory access
10 register comprising a command register comprising a compare enable bit and a branch enable bit.

1 Claim 7. (*Withdrawn*) A system as in claim 6, said direct memory access register further
2 comprising a source address register and a target address register.

1 Claim 8. (*Withdrawn*) A system as in claim 7, wherein said compare enable bit is adapted
2 to indicate a comparison operation to be performed by said direct memory access controller
3 based on said source address register and said target address register.

1 Claim 9. (*Withdrawn*) A system as in claim 6, wherein said branch enable bit is adapted
2 to indicate a branch operation to be performed by said direct memory access controller to fetch

3 said fourth descriptor or said third descriptor from said memory.

1 Claim 10. (*Withdrawn*) A system as in claim 9, wherein said first descriptor is adapted to
2 indicate data transfer by said direct memory access controller, and wherein said third descriptor
3 is adapted to indicate no data transfer by said direct memory access controller.

1 Claim 11. (*Withdrawn*) A system as in claim 6, said direct memory access controller
2 further comprising a control status register, said control status register comprising a compare
3 status bit.

1 Claim 12. (*Withdrawn*) A system as in claim 11, wherein said branch enable bit is
2 adapted to indicate a branch operation to be performed by said direct memory access controller
3 to fetch said fourth descriptor or said third descriptor from said memory based on said compare
4 status bit.

1 Claim 13. (*Withdrawn*) A system as in claim 11, wherein said direct memory access
2 controller is adapted to perform a comparison operation and a branch operation based on said
3 branch enable bit, said comparison enable bit, and said compare status bit.

1 Claim 14. (*Withdrawn*) A machine-readable medium that provides instructions, which
2 when executed by a computing platform, cause said computing platform to perform operations
3 comprising a method of:
4 fetching a first descriptor of a first type, said first descriptor identifying a first source and

5 a first target;
6 transferring a first data set over a direct memory access channel from said first source to
7 said first target based on said first descriptor;
8 fetching a second descriptor of a second type, said second descriptor identifying a second
9 source, said second descriptor comprising comparison data;
10 fetching data from said second source identified by said second descriptor;
11 comparing said data fetched from said second source and said comparison data to obtain
12 a comparison result; and
13 fetching one of a fourth descriptor of said first type and a third descriptor of a third type
14 based on said comparison result.

1 Claim 15. (*Withdrawn*) A machine-readable medium as in claim 14, wherein said fourth
2 descriptor is fetched if said comparison result indicates said data fetched from said second source
3 fails to match said comparison data.

1 Claim 16. (*Withdrawn*) A machine-readable medium as in claim 14, wherein said third
2 descriptor is fetched if said comparison result indicates said data fetched from said second source
3 matches said comparison data.

1 Claim 17. (*Withdrawn*) A machine-readable medium as in claim 14, wherein said second
2 descriptor comprises a branch enable bit and a comparison enable bit, wherein said comparing
3 data fetched is based on said comparison enable bit in said second descriptor, and said fetching
4 one of said fourth descriptor and said third descriptor is based on said branch enable bit in said

5 second descriptor.

1 Claim 18. (*Withdrawn*) A machine-readable medium as in claim 14, wherein said data
2 fetched from said second source comprises a transfer status indicator.

1 Claim 19. (*Withdrawn*) A method, comprising:
2 fetching a first descriptor of a first type, said first descriptor identifying a first source and
3 a first target;
4 transferring a first data set over a direct memory access channel from said first source to
5 said first target based on said first descriptor;
6 fetching a second descriptor of a second type, said second descriptor identifying a second
7 source, said second descriptor comprising comparison data;
8 fetching data from said second source identified by said second descriptor;
9 comparing said data fetched from said second source and said comparison data to obtain
10 a comparison result; and
11 fetching one of a fourth descriptor of said first type and a third descriptor of a third type
12 based on said comparison result.

1 Claim 20. (*Withdrawn*) A method as in claim 19, wherein said fourth descriptor is fetched
2 if said comparison result indicates said data fetched from said second source fails to match said
3 comparison data.

1 Claim 21. (*Withdrawn*) A method as in claim 19, wherein said third descriptor is fetched

- 2 if said comparison result indicates said data fetched from said second source matches said
- 3 comparison data.

1 Claim 22. (*Withdrawn*) A method as in claim 19, wherein said second descriptor
2 comprises a branch enable bit and a comparison enable bit, wherein said comparing data fetched
3 is based on said comparison enable bit in said second descriptor, and said fetching one of said
4 fourth descriptor and said third descriptor is based on said branch enable bit in said second
5 descriptor.

1 Claim 23. (*Withdrawn*) A machine-readable medium as in claim 19, wherein said data
2 fetched from said second source comprises a transfer status indicator.